IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Appl. No. | : | 09/546,174 | Confirmation No.: 4793 |
| Applicant | : | Chih-Chien Liu | |
| Filing Date | : | April 11, 2000 | |
| Title | : | HIGH DENSITY PLASMA CHEMICAL VAPOR DEPOSITION PROCESS | |
| Group Art Unit | : | 1796 | |
| Examiner | : | Sergent, Rabon A. | |
| Docket No. | : | 20952.4002 | |
| Customer No. | : | 34313 | |

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT IN RESPONSE TO FINAL OFFICE ACTION

Sir:

Applicants filed a Notice of Appeal on June 13, 2008 in response to the Final Office Action dated March 13, 2008, so that this amendment is timely filed. Please amend the above-identified application as follows:

Amendments to the claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 10 of this paper.

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1-49. (Canceled)

50. (Previously Presented) A method for forming conducting structures separated by gaps on a substrate comprising:

providing a substrate and a wiring line layer above the substrate;

providing a conductive layer on the wiring line layer;

forming a cap layer directly on the conductive layer, wherein the cap layer has a particular thickness to create destructive interference and the cap layer has a composition adapted to provide a graded index of refraction between said conductive layer and a photoresist layer during a photolithographic process, the photoresist layer being formed on top of the cap layer;

etching through a portion of the cap layer and portions of the conductive layer and wiring line layer to form wiring lines separated by gaps, the wiring lines having a remaining portion of the cap layer thereon; and

depositing a dielectric material on surfaces exposed by the etching process including exposed surfaces of the cap layer to substantially fill the gaps between the wiring lines, said dielectric material including a layer formed by high density plasma chemical vapor deposition,

wherein the cap layer acts to protect the wiring lines and portions of the cap layer are sacrificially removed during the process of depositing the dielectric material.

51. (Previously Presented) The method of claim 50, wherein the cap layer is used as a hard mask during etching of the wiring line layer prior to when portions of the cap layer are sacrificially removed during the process of depositing the dielectric material.

52. (Previously Presented) The method of claim 50, wherein the cap layer comprises an antireflective coating that operates by destructive interference, and said conductive layer comprises a layer of titanium nitride.

53. (Previously Presented) The method of claim 50, wherein the cap layer comprises an oxynitride antireflective coating and said conductive layer comprises a metallic layer comprising titanium above a layer comprising aluminum.

54. (Previously Presented) The method of claim 50, wherein the cap layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, or silicon oxynitride.

55. (Previously Presented) The method of claim 50, wherein the remaining portion of the cap layer on at least one wiring line has a rectangular shape in cross section prior to when portions of the cap laver are sacrificially removed during the process of depositing the dielectric material.

56. (Previously Presented) The method of claim 50, wherein the remaining portion of the cap layer on at least one wiring line has a trapezoidal shape in cross section.

57. (Previously Presented) The method of claim 56, wherein the trapezoidal shape includes top and bottom surfaces parallel to one another and side surfaces that extend inwardly from the bottom surface to the top surface.

58. (Previously Presented) The method of claim 50, wherein the remaining portion of the cap layer on at least one wiring line has a triangular shape in cross section.

59. (Previously Presented) The method of claim 50, wherein the remaining portion of the cap layer on at least one wiring line has, in cross section, a rectangular shape having its upper corners etched away.

60. (Previously Presented) The method of claim 50, wherein the remaining portion of the cap layer is shaped using etching prior to the depositing a dielectric material to have a shape that reduces redeposition of the cap layer into the gaps during the high density plasma chemical vapor deposition process.

61. (Previously Presented) A method of forming conducting structures separated by gaps filled with dielectric material, the method comprising:

providing a substrate containing silicon, the substrate having a surface;

forming a surface layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium tungsten alloy, the surface layer disposed on the substrate surface;

forming a metal wiring layer on the surface layer, the metal wiring layer having an upper surface;

forming a protective layer comprising at least one layer of a material selected from the group consisting of titanium nitride, titanium silicide and a titanium-tungsten alloy, the protective layer disposed on the upper surface of the metal wiring layer, the protective layer having a top surface;

forming a cap layer comprising at least one material selected from the group consisting of an oxide, a nitride, a silicon-rich oxide, and an oxynitride, the cap layer disposed directly on the top surface of the protective layer, wherein said cap layer has a particular thickness to create destructive interference and a composition, the particular thickness and the composition adapted so that at least during a photolithographic process said cap layer creates destructive interference to reduce reflections;

forming a patterned photoresist layer on the cap layer, said patterned photoresist layer covering selected portions of the cap layer and exposing other portions of the cap layer;

etching the cap layer, the protective layer and the metal wiring layer to form the conductive structures separated by gaps; and

depositing dielectric material, including depositing at least a portion of dielectric material using high density plasma chemical vapor deposition (HDPCVD) on surfaces exposed by the etching process including exposed surfaces of the cap layer, wherein the gaps are substantially filled with the dielectric material, and

wherein the cap layer acts to protect the wiring lines and portions of the cap layer are sacrificially removed during the process of forming the dielectric material on surfaces exposed by the etching process, wherein the protective layer comprises a material having a first dielectric constant and the cap layer comprises an antireflective coating having a second dielectric constant, different from the first dielectric constant, and wherein the first dielectric constant and the second dielectric constant form a graded index of refraction.

62. (Previously Presented) The method of claim 61, wherein the cap layer is used as a hard mask during etching of the wiring line layer.

63. (Previously Presented) The method of claim 61, wherein portions of the cap layer are etched during the depositing dielectric material using high density plasma chemical vapor deposition.

64. (Previously Presented) The method of claim 61, wherein the cap layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, or silicon oxynitride.

65. (Previously Presented) The method of claim 61, wherein the depositing dielectric material using high density plasma chemical vapor deposition substantially fills the gaps between the conductive structures.

66. (Previously Presented) The method of claim 61, wherein the dielectric material is deposited using high density plasma chemical vapor deposition onto a surface of

the substrate, onto side surfaces of the metal wiring layer, the surface layer, the protective layer, and the cap layer.

67. (Previously Presented) The method of claim 61, wherein the dielectric material is deposited using high density plasma chemical vapor deposition onto an upper surface of the cap layer.

68. (Previously Presented) The method of claim 61, further comprising removing the patterned photoresist layer prior to depositing the dielectric material using high density plasma chemical vapor deposition.

69. (Previously Presented) The method of claim 61, wherein the cap layer protects the underlying wiring layer throughout the depositing the dielectric material using high density plasma chemical vapor deposition.

70-71. (Canceled)

72. (Previously Presented) The method of claim 61, wherein the graded index of refraction reduces boundary reflections between the protective layer and the antireflective coating.

73. (Canceled)

74. (Previously Presented) The method of claim 61, wherein twice the particular thickness of the cap layer is an odd number of the wavelengths of the exposure light, compensating for the dielectric constant of the cap layer.

75-79. (Canceled)

80. (Previously Presented) A method for forming conducting structures separated by gaps on a substrate comprising:

providing a substrate and a wiring line layer above the substrate;

forming a first antireflective coating above the wiring line layer;

forming a cap layer adapted for protecting the wiring line layer during a plasma based process, the cap layer being situated directly on the first antireflective coating and having a particular thickness to create destructive interference, wherein the cap layer and the first antireflective coating have different dielectric constants;

forming a photoresist layer directly on top of the cap layer;

patterning the photoresist layer during a lithographic process;

etching through portions of the first antireflective coating, a portion of the cap layer and a portion of the wiring line layer to form wiring lines separated by high aspect ratio gaps; and

depositing a dielectric material to substantially fill the gaps, including using a HDPCVD process at least until any high aspect ratio gaps are substantially filled, followed by a different plasma process that fills any remaining portion of said gaps and results in a planarized surface,

wherein the cap layer and the first antireflective coating form a graded change in an index of refraction.

81. (Previously Presented) The method of claim 80, wherein the first antireflective coating absorbs portions of radiation applied during the lithographic process.

82. (Previously Presented) The method of claim 80, wherein the cap layer also functions as a mask during the etching process.

83. (Previously Presented) The method of claim 80, wherein an additional portion of the cap layer is etched while the cap layer protects the wiring line layer during the HDPCVD process.

84. (Previously Presented) The method of claim 80, further comprising forming a surface layer between the substrate and the wiring line layer.

85. (Previously Presented) The method of claim 80, further comprising the step of removing the cap layer before depositing a dielectric material within the gaps.

86. (Previously Presented) The method of claim .80, wherein portions of the cap layer are removed and portions of the cap layer act as a mask during the etching of the first antireflective coating and the wiring line layer.

87. (Previously Presented) The method of claim 80, wherein after etching each wiring line has a portion of the cap layer thereon, the portion of a cap layer on each wiring line having a cross-sectional shape selected from the group consisting of a rectangle, a triangle, trapezoid, and a rectangle having its upper corners etched away.

88. (Previously Presented) The method of claim 80 wherein the cap layer and the first antireflective coating are used as a hard mask.

89. (Canceled)

90. (Previously Presented) The method of claim 80 wherein the cap layer has a dielectric constant that is closer to a dielectric constant of the first antireflective coating than to the photoresist mask layer dielectric constant.

91. (Previously Presented) The method of claim 80, wherein said different plasma process deposits material at a higher rate than the HDPCVD process.

92. (Previously Presented) The method of claim 80, wherein said different plasma process is a PECVD oxide process.

93. (Previously Presented) The method of claim 80, wherein the cap layer comprises silicon, oxygen, and nitrogen.

94-97. (Canceled)

98. (Previously Presented) The method of claim 50, wherein the cap layer comprises silicon-rich oxide.

99. (Previously Presented) The method of claim 80, wherein the cap layer comprises silicon-rich oxide.

100. (Previously Presented) The method of claim 50, wherein a portion of the substrate is etched when the wiring lines are etched.

101. (Previously Presented) The method of claim 61, wherein a portion of the substrate is etched when the wiring lines are etched.

102. (Previously Presented) The method of claim 80, wherein a portion of the substrate is etched when the wiring lines are etched.

## Remarks

This after-final amendment is filed within two months of the filing of a Notice of Appeal and before filing the Appeal Brief in this application. Claims 50-69, 72, 74, 80-88, 90-93 and 98-102 are pending in this application. Claims 1-49, 70-71, 73, 75-79, 89 and 94-97 have been cancelled without prejudice.

I. Formalities

Applicants respectfully request that the attorney docket number for the present application be changed from Docket No. JIA 462C1 to Docket No. 20952.4002.

II. Claim Cancellation

Applicants cancel claims 94-97 to simplify issues on appeal. Entry of this amendment is requested on that basis.

III. Conclusion

Entry of the above-referenced amendments is requested to place the application in better condition for the appeal. Should the Examiner have any questions or comments, the undersigned can be reached at (213) 612-2478.

The Commissioner is authorized to charge any fee which may be required in connection with this Amendment to deposit account No. 15-0665.

Respectfully submitted,
ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: 12 August 2008

By: _____
William H. Wright
Reg. No. 36,312

Orrick, Herrington & Sutcliffe LLP
777 S. Figueroa Street, Suite 3200
Los Angeles, CA 90017-5855
Tel. 213-612-2478
Fax: 213-612-2499